REMARKS

By this amendment, claims 1, 3-4, 6-8, 10, 20, 22, 26, 31, and 33 have been amended. Claims 2, 21, and 32 have been canceled. Claims 1, 3-20, 22-31, and 33-36 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 1-2, 6, 10, 13-14, 16, 18, 20-21, 25-28, and 31-32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Pain et al. (US WO 99/48281). This rejection is respectfully traversed.

Claim 1, as amended, recites an image sensor readout circuit comprising, *inter alia*, "a binning circuit ... [which] comprises: a first plurality of charge storage devices for respectively storing a predetermined plurality of analog pixel signals from a plurality of pixels, a first combining circuit for combining said stored plurality of analog pixel signals and outputting them on a first output line, a second plurality of charge storage devices for respectively storing a predetermined plurality of analog reset signals from a plurality of pixels, and a second combining circuit for combining said stored plurality of analog reset signals and outputting them on a second output line" (emphasis added). Pain et al. does not disclose these limitations.

To the contrary, Pain et al. discloses only capacitor CIS which combines pixel signals, and capacitor CIR which combines reset signals, but does not disclose storing each signal, then combining the separate stored signals and outputting them. Pain et al. FIG. 2A. Applicant respectfully submits that Pain et al. does disclose, teach, or suggest a first and second plurality of charge storage devices for respectively storing a predetermined plurality of analog and reset signals from a plurality of pixels and a first and second combining circuit for combining the stored plurality of analog and reset

signals as recited in claim 1. Since Pain et al. does not disclose all the limitations of claim 1, claim 1 and dependent claim 2 are not anticipated by Pain et al.

Claim 6 recites a binning circuit comprising, *inter alia,* a "first sample circuit comprising a first plurality of charge storage devices respectively storing a plurality of analog pixel signals from a plurality of pixels; [and a] second sample circuit comprising a second plurality of charge storage devices respectively storing a plurality of analog reset signals from a plurality of pixels; a first switch ... being controlled to combine said stored plurality of analog pixel signals and output said combined pixel signals on said first output line; and a second switch ... being controlled to combine said stored plurality of analog reset signals and output said combined reset signal on said second output line" (emphasis added). Pain et al. does not disclose these limitations.

To the contrary, Pain et al. discloses only capacitor CIS which combines pixel signals, and capacitor CIR which combines reset signals, but does not disclose storing each signal, then combining the separate stored signals and outputting them. Pain et al. FIG. 2A. There is no first and second sample circuit comprising a first and second plurality of charge storage devices respectively storing a plurality of analog pixel and reset signals from a plurality of pixels and a first and second switch being controlled to combine said stored plurality of analog pixel and reset signals as recited in claim 6. Since Pain et al. does not disclose all the limitations of claim 6, claim 6 is not anticipated by Pain et al.

Claim 10, as amended, recites a method of binning the output of an active image sensor comprising, *inter alia,* "sampling and respectively storing analog output signals from a plurality of pixels of said sensor according to a first predetermined sequence; sampling and respectively storing analog reset signals from a plurality of pixels of said sensor according to a second predetermined sequence; subsequently combining and

outputting all sampled and stored analog output signals on a first line; and combining and outputting all sampled and stored analog reset signals on a second line" (emphasis added). Pain et al. does not disclose these limitations.

To the contrary, Pain et al. discloses only capacitor CIS which combines pixel signals, and capacitor CIR which combines reset signals, but does not disclose storing each signal, then combining the separate stored signals and outputting them. Pain et al. FIG. 2A. Applicant submits that Pain et al. does not disclose sampling and respectively storing analog output and reset signals from a plurality of pixels and subsequently combining the sampled and stored analog output and reset signals as recited in claim 10. Since Pain et al. does not disclose all the limitations of claim 10, claim 10 and dependent claims 13-14, 16, and 18 are not anticipated by Pain et al.

Claims 20 and 31, as amended, recite a charge-domain readout circuit comprising, inter alia, "a plurality of column readout circuits each of which sample and combine multiple pixel signals and reset signal values of a plurality of pixels of an active pixel sensor, wherein each column readout circuit is associated with a respective column of sensors in said active pixel sensor, each of said plurality of column readout circuits comprising: a plurality of charge storage devices for respectively storing each of said multiple pixel signals and reset signal values, and a combining circuit for combining said respectively stored multiple pixel signals and reset signal values" (emphasis added). Pain et al. does not disclose these limitations.

To the contrary, Pain et al. discloses only capacitor CIS which combines pixel signals, and capacitor CIR which combines reset signals, but does not disclose storing each signal, then combining the separate stored signals and outputting them. Pain et al. FIG. 2A. There is no plurality of column readout circuits comprising a plurality of charge storage devices for respectively storing each of said multiple pixel signals and

reset signal values, and a combining circuit for combining said respectively stored multiple pixel signals and reset signal values as recited in claims 20 and 31. Since Pain et al. does not disclose all the limitations of claims 20 and 31, claims 20 and 31 are not anticipated by Pain et al. Claims 21 and 25 depend from claim 20 and are patentable at least for the reasons mentioned above. Claim 32 depends from claim 32 and is patentable at least for the reasons mentioned above.

Claim 26 recites a method of reading out values from active pixel sensors comprising, *inter alia*, "storing correlated double sampled values for a plurality of sensors in said selected rows, wherein said values for each sensor are stored by a respective pair of charge storage devices in a readout circuit associated with a column in said array in which said sensor is located; [and] combining said stored signals" (emphasis added). Pain et al. does not disclose these limitations.

To the contrary, Pain et al. discloses only capacitor CIS which combines pixel signals, and capacitor CIR which combines reset signals, but does not disclose storing each signal, then combining the separate stored signals and outputting them. Pain et al. FIG. 2A. There is no storing correlated double sampled values for a plurality of sensors by a respective pair of charge storage devices and combining said stored signals as recited in claim 26. Since Pain et al. does not disclose all the limitations of claim 26, claim 26 and dependent claims 27-28 are not anticipated by Pain et al.

Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection be withdrawn and claims 1-2, 6, 10, 13-14, 16, 18, 20-21, 25-28, and 31 be allowed.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Pain et al. This rejection is respectfully traversed. Claim 19 depends from claim 10 and is patentable at least for the reasons mentioned above. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 19 be withdrawn.

Claims 15 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pain et al. in view of Okamoto (US 2003/019580). This rejection is respectfully traversed. Claims 15 and 17 depend from claim 10 and are patentable at least for the reasons mentioned above. Okamoto, which has been cited as allegedly teaching sampling colors that take into account a Bayer pattern, fails to cure the above noted deficiencies of Pain et al. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 15 and 17 be withdrawn.

Claims 3-5, 7-9, 11-12, 22-24, 30, and 33-36 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. Claims 3-5, 7-9, 11-12, 22-24, 30, and 33-36 depend, respectively, directly, or indirectly from independent claims 1, 6, 10, 20, 26, and 31, and are allowable for at least the reasons set forth above.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

Dated: April 17, 2006

Respectfully submitted,

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